## REMARKS

Claims 1-7 are pending the above-referenced application. Claims 1-7 are rejected in the current Office Action. The drawings are accepted and the Action is non-final. In particular and according to the item number therein, the Office Action has:

In Items 2 through 5, rejected claims 1, 4-5, and 7 under 35 U.S.C. 102(e) as being anticipated by Pavisic (U.S. Patent No. 6,550,044);

In Items 6 through 8, rejected claims 1, 4-5, and 7 under 35 U.S.C. 102(e) as being anticipated by Graef (U.S. Patent No. 6,189,131); and

In Items 9 through 12, rejected claims 2-3 and 6 under 35 U.S.C. 102(e) as being obvious over Pavisic '044, in view of Hathaway (U.S. Patent No. 5,963,728) and Graef '131) and further in view of Arnold (U.S. 6,099,548).

Applicants have amended claims 2, 3, 4, and 6 and corrected minor diction errors in paragraph 10 of Applicants' specification.

In Item 4, regarding claim 1, the Office Action has rejected that claim under 35 U.S.C. 102(e) as being anticipated by Pavisic. The Pavisic reference describes a method of synthesizing a clock tree. Pavisic performs this method, according to the flow chart of FIG. 4 or FIG. 5. According to the flow charts of FIGs. 4 and 5, an initial balanced clock tree is constructed and an arrival time is calculated for each flip-flop in the initial clock tree. After this a timing analysis is performed and a skew optimization is performed. The skew optimization is each figure is slightly different but amounts to putting a buffer of a certain size in the clock path to reduce the timing violations discovered by the timing analysis. Pavisic '044, Co. 4, lines 19-21. In FIG. 4, an additional step of compensating for any hold time violations occurs by placing a buffer in the signal path. However, the Pavisic reference is silent about "performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects," because Pavisic fails to prioritize the timing violations according to their size of timing violation. According to the Pavisic reference all timing

violations are the same, i.e., the size of the violation is not a factor. The portion of Pavisic cited in support of the Office Action's arguments describes briefly the process of skew optimization but does not address the issue of determining which are the largest timing violations. Therefore, the Pavisic fails to teach each and every limitation in claim 1. Because the same limitation is present in claim 5 and claim 7, Pavisic fails to teach each and every limitation of these claims as well.

In Item 5, with respect to claim 4, Applicants submit that claim 4 is allowable at least because claim 1 is allowable.

In Items 6 and 7, The Office Action has rejected claims 1, 4-5 and 7 as anticipated by Graef. The Graef reference describes a method for using layer specific wire load models in the synthesis and layout of integrated circuits. Graef '131, Col. 2, lines 49-51. The Graef reference briefly mentions the correction of timing violations at Col. 7, lines 49-54, by means of an In-Place Optimization. However, Graef is completely silent about "identifying components or interconnects of the network that have the highest amount of timing violation potential." Therefore, Applicants believe that Graef fails to teach each and every limitation of claim 1, and because claims 5 and 7 have the same limitations, those claims as well.

In Item 8, with respect to claim 4, Applicants submit that claim 4 is allowable at least because claim 1, from which it depends is allowable.

In Items 9 through 12, The Office Action has rejected claims 2-3 and 6 under 35 U.S.C. 102(e) as being obvious over Pavisic '044, in view of Hathaway (U.S. Patent No. 5,963,728) and Graef '131) and further in view of Arnold (U.S. 6,099,548).

The Hathaway reference describes a method of building clocking circuitry of an IC. Hathaway '728, Abstract. The Arnold reference describes a design tool that includes a timing verifier, a placement tool, and an in-place optimization tool. The Office Action alleges that the proposed combination of Pavisic, Graef, Hathaway and Arnold would have resulted in Applicants' invention. However, the combination of references does not teaches the limitation "performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects." As described above, neither Pavisic nor Arnold teach this limitation, and neither Hathaway nor Arnold describes

anything about identifying components in a network that have the highest amount of timing violation potential and executing an in-place optimization according to the *identified* components or interconnects. Therefore, the combination of references fails to teach all of the limitations of claims 1, 5 and 7. Claims 2 and 6 are dependent claims that recite the steps, in one embodiment, of performing the selective in place optimization. The combination of references fails further to teach the limitation "performing logic operations to generate a selection list of selected components or nets or both with the greatest amount of timing violation potential based on the user-provided criteria and removing clock nets from the selection list." The Hathaway reference describes a method of constructing a clock network and mentions nothing about performing a timing analysis. The goal of the algorithm disclosed in the reference is to find the minimum wire length solution with every net having substantially equal net loadings within given limits. Hathaway '728, Col. 2, lines 12-16. As such, the method disclosed in the Hathaway reference has no bearing on in place optimizations; it is more concerned with initial layout and subsequent refinement of that initial layout to achieve the above stated goal as closely as possible. The above stated goal is not a timing goal, it is a loading goal. The Arnold reference does mention a timing analysis, but that analysis does not describe the limitations of claim 2. The reference states an object of the invention as having the possibility of running an in place optimization within a placement tool to fix high level timing constraints violations. Arnold '584, Col. 3, lines 27-30. In fact, at one place in the Arnold reference, it states that if the designer encounters a condition where the slacks are very negative, then the designer should essentially give up as the IPO will not solve the problem. Arnold '584, Col. 4, lines 32-35. Applicants invention, by dealing with components or nets with the largest timing violation potential, expects that the worst negative slack will be greatly reduced. Applicants' specification, page 4. Thus, Applicants' invention deals with a condition that the Arnold reference teaches cannot be handled by in place optimization. Thus, the Arnold reference fails to teach or suggest a timing analysis which has the limitation "performing logic operations to generate a selection list of selected components or nets or both with the greatest amount of timing violation potential based on the user-provided criteria and removing clock nets from the selection list; and performing an in-place optimization with only the selected components or nets or both."

As a result, Applicants conclude that the combination of references fails to teach or suggest all of the limitations of claims 2 and 6 and fails to suggest any modification of the references that would meet the limitations of claims 2 and 6.

With respect to claim 3, the combination of references fails to teach the limitation "wherein the selected components or nets with greatest amount of timing violation potential are stored in a Net File," because the combination fails to teach the limitation that "selected components or nets with the greatest amount of timing violation potential are stored."

The Office Action has cited portions of each reference in support of the obviousness allegation. The cited portion of Pavisic describes the conditions in FIG. 1 that lead to a timing violation, the insertion of a clock buffer to remove the timing violation. FIGs. 3 and 4 of Graef show the flowcharts of a design methodology using multi-layer wire load information. The Summary of the invention portion describes the inclusion of wire load models in a technology library, which permits more accurate timing estimates than generic wire delay values. Column 4 of Graef describes FIG. 2 which shows multiple layers of wire interconnected with vias. It also describes the specific nature of the wire load models, ones that include capacitance per unit length, resistance per unit length values, and via and contact resistance and capacitance values. Col. 5, lines 32-67 of the Graef reference describe how the synthesis tools of the present invention use the multi-layer wire load information to produce more accurate timing estimates than those that can be realized with generic values. Col. 6, lines 1-25 of the Graef reference describe the use of delay calculators to perform a static timing analysis of the design. Col. 7, lines 1 through Col. 8, line 12 describes mostly the steps of FIG. 4 and suggests that an in place optimization be performed in step 338. FIG. 4 of Arnold describes a flow which mentions in place optimization and a timing check. FIGs. 5 and 6 of Arnold describes a flow in which a timing report is generated. Applicants fail to understand how these teachings would have resulted in Applicants' invention. Nothing in these teachings suggests the removal of the clock nets from the selection list as recited in claims 2 and 6 and nothing in these teachings suggest "performing logic operations to generate a selection list of selected components or nets or both with the greatest amount of timing violation potential based on the user-provided criteria," as recited in claims 2 and 6.

Furthermore, Applicants respectfully submit that one of ordinary skill in the art would not have made the combination proposed in the Office Action. It is not clear from the teachings of the Pavisic reference why one of skill in the art would have turned to the Graef reference. Pavisic deals with the correction of timing violations in a clock tree. Graef deals with the inclusion of proper interconnect wire load models that are layer dependent in the library. Nothing in Pavisic suggests the need for having better wire load models. Therefore, Applicants respectfully submit that the proposed combination would not have been made by one of ordinary skill in the art.

Finally, with respect to claim 3 in Item 12, Applicants respectfully submit that Graef fails to teach the limitation "wherein the selected components or nets with greatest amount of timing violation potential are stored in a Net File," because Graef says nothing about selecting components or nets with the greatest amount of timing violation. The cited portion of Graef does mention static timing analysis and formats of files, including netlists, but there is no mention of what is in those files, specifically, selected components or nets with the greatest amount of timing violation potential. Therefore, the cited portion of Graef does not supply the limitation recited in claim 3.

Thus, having responded to each and every ground of rejection and objection, Applicants respectfully request reconsideration and allowance of the pending claims and the new claims in the above-mentioned application.

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Respectfully submitted

Anthony B. Diepenbrock III
Reg. No. 39,960
Attorney for Applicant
(650) 813-4856

DECHERT LLP
1117 California Avenue
Palo Alto, CA 94304
Tel: (650) 813-4800
Fax: (650) 813-4848

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**Date: August 8, 2005**

Sushma S. Brady

**Sushma S. Brady**